HDL modeling

1. Gate level ( lowest level of abstraction ) ( Structural modeling )

* Example : And a1(y,a,b) ;

1. Switch level

* pmos p1(y,vdd,x);
* nmos n1(y,and,x);

1. Data flow modeling ( methods of abstraction )

* Assign y = a ^b;

1. Behavioral modeling ( highest level of abstraction )

* Procedural constructor (block)
* Always – sequential block
* initial
* = : blocking
* <= : non-blocking
* Every sequential is non-blocking
  + - Structure queue
      * Active queue
        + Contininue assignment student , assign y = ( a|b)
        + = -> y = a&b;
        + $display = > $display (y);
        + RHS express is NBA structure
        + $monitor
        + $ strobe